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DICKE, BILLIG & CZAJA, FIFTH STREET TOWERS 100 SOUTH FIFTH STREET, SUITE 2250 MINNEAPOLIS, MN 55402			TRAN, KHAI	
			ART UNIT	PAPER NUMBER
			2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/786,879

Applicant(s)

PARTOVI ET AL.

Examiner

KHAI TRAN

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 July 0207.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8-21 is/are allowed.
- 6) ☒ Claim(s) 1,5 and 22-28 is/are rejected.
- 7) ☒ Claim(s) 2-4,6 and 7 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. The amendment filed 7/6/2007 has been entered. Claims 1-28 are pending in this Office action.

Response to Arguments

2. Applicant's arguments filed 7/6/2007 have been fully considered but they are not persuasive.

Applicant argues in page 9 of the Remarks that the CDR circuit 50 as taught by Aung et al does not have a clock source input coupled to the serial data input of the CDR circuit 50, and in particular, the CDR circuitry 50 is not responsive to a clock source signal received at the serial data input thereof for producing a desired clock signal as recited in claim 1.

Response to the Applicant's argument that the CDR 50 has a clock source (CDR signal source 20) coupled to the serial data input of the CDR circuit 50. The CDR circuitry 50 is responsive to a clock source signal from the clock source (CDR signal source 20) for producing a desired clock signal (see [0069]- [0070]).

Applicant argues that Figure 7 of Aung et al fail to disclose any CDR circuitry in the transmitter.

Examiner mistakenly indicated the Figure 7, it should have been Figure 1, which shows a receiver having a CDR circuitry (50) for receiving the clock source signal. Examiner appreciates for pointing out this error.

Claim Rejections - 35 USC § 102

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3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 5, 22-23, 25-28 remain rejected under 35 U.S.C. 102(e) as being anticipated by Aung et al (US 2003/0212939 A1).

Regarding claim 25, Aung et al disclose a serial data transceiver apparatus, comprising: means for deserializing (60) an input serial data stream (Figure 1); means for converting parallel data (see Figure 7, a serializer 340) into output serial data stream based on a transmit serialization clock signal; means for producing the transmit serialization clock signal by applying a CDR (a CDR 50) operation to a clock source signal (a reference clock signal source 22).

Regarding claim 26, Aung et al disclose a receive data input for receiving an input serial data stream (a receiver 40); a clock and data recovery (CDR) circuit (50) coupled to the receive data input for recovering a receive clock signal from the input serial data stream; a data serializer (340) for converting parallel data into an output serial data stream, the data serializer having a clock input for receiving a transmit serialization clock signal (from a PLL 100), the data serializer (340) for producing the output serial data stream based on the transmit serialization clock signal; a clock synthesizer apparatus (a reference clock signal source 22) coupled to the clock input for

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providing the transmit serialization clock signal; the CDR circuit (50) and clock synthesizer having respective PLL clock inputs, each the PLL clock input for receiving first and second PLL clocks (see Figure 7 shows the PLL circuit having two clock output signals; a PLL (100) having an output for providing the first and second PLL clocks, the CDR circuit and the synthesizer apparatus (22) each having said PLL clock input thereof coupled to the PLL output for receiving the first and second PLL clocks.

Claims 27-28 are similar to claim 25. Therefore, claims 27-28 are rejected under a similar rationale.

Claims 22-23 are similar to claim 25. Therefore, claims 22-23 are rejected under a similar rationale.

Claims 1, 5 are similar to claims 25-26. Aung et al further disclose a clock source input for receiving a clock source signal having a fixed transition density (see [0036], a reference clock signal source 22 can produce a reference clock signal having the same frequency as the clock frequency embedded in the CDR data signal or any convenient fraction or multiple of the embedded frequency). Therefore, claims 1, 5 are rejected under a similar rationale.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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6. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aung et al in view of the admitted prior art.

Regarding claim 24, Aung et al fail to disclose a step of filtering the clock source signal in the digital domain. However, the admitted prior art discloses that the noisy external clock source typically cleaned up by applying thereto a narrow-band filtering operation (page 2, lines 6-8). It would have been obvious to one having ordinary skill in the art at the time the invention was made to filter the clock source signal as taught by the admitted prior art into the teachings of Aung et al in order filter out unwanted noise.

Allowable Subject Matter

7. Claims 8-21 are allowed.

8. Claims 2-4, 6-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter: Aung et al fail to disclose or suggest that a clock synthesizer comprising a second CDR circuit having a serial data input, said second CDR circuit operable when a serial data stream is applied thereto via said serial data input for recovering a clock signal from the serial data stream, said clock synthesizer apparatus including a clock source input for receiving a clock source signal, said clock source input coupled to said serial data input for applying said clock source signal to said second CDR circuit, said second CDR circuit responsive to said clock source signal for producing said transmit

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serialization clock signal; and a transmit data output coupled to said data serializer for transmitting said output serial data stream.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KHAU TRAN whose telephone number is (571) 272-3019. The examiner can normally be reached on 7:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on (571) 272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



KHAI TRAN
Primary Examiner
Art Unit 2611

KT
06 September, 2007